

I CLAIM:

1. A method of configuring a memory controller, said memory controller having a plurality of input/output pins, said method comprising:

5 informing said memory controller of a type of memory; and

 configuring at least one said pin to have a functionality in accordance with said type of memory.

10 2. The method of claim 1 wherein said type of memory is a buffered memory.

 3. The method of claim 1 wherein said type of memory is an unbuffered memory.

15 4. The method of claim 1 wherein said configuring comprises configuring said functionality of said pin to a clock signal function.

 5. The method of claim 4 wherein said clock signal function is a differential clock signal function.

20 6. The method of claim 1 wherein said configuring comprises configuring said functionality of said pin to a chip select signal function.

25 7. The method of claim 1 wherein said functionality of said pin is one of a chip select signal function and a clock signal function.

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8. A method of providing more than one function for an output pin of a memory controller, said method comprising:

5 providing a clock signal within said memory controller;

providing a control signal within said memory controller;

10 selecting within said memory controller one of said clock signal and said control signal based on a type of memory; and

coupling said selected signal to said output pin.

9. The method of claim 8 wherein said type of memory is a buffered memory.

15 10. The method of claim 8 wherein said type of memory is an unbuffered memory.

11. The method of claim 8 wherein said clock signal is a differential clock signal.

12. The method of claim 8 wherein said 20 control signal is a chip select signal.

13. A memory controller comprising:
at least one output pin;
a multiplexer having two inputs, a
control input, and an output coupled to said output
25 pin;

a chip select signal coupled to one of
said two inputs;

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a control signal coupled to the other one of said two inputs; and

5 a signal coupled to said control input that selects one of said chip select signal and said control signal based on a type of memory.

14. The memory controller of claim 13 wherein said type of memory is a buffered memory.

15. The memory controller of claim 13 wherein said type of memory is an unbuffered memory.

10 16. The memory controller of claim 13 wherein said control signal is a clock signal.

17. The memory controller of claim 16 wherein said clock signal is a differential clock signal.

15 18. A memory controller comprising:
at least one output pin;

a multiplexer having two inputs, a control input, and an output coupled to said output pin;

20 a clock signal coupled to one of said two inputs;

a control signal coupled to the other one of said two inputs; and

25 a signal coupled to said control input that selects one of said clock signal and said control signal based on a type of memory.

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19. The memory controller of claim 18
wherein said type of memory is a buffered memory.

20. The memory controller of claim 18
wherein said type of memory is an unbuffered memory.

5 21. The memory controller of claim 18
wherein said control signal is a chip select signal.

22. The memory controller of claim 18
wherein said clock signal is a differential clock
signal.

10 23. A memory controller comprising:
at least one output pin; and
circuitry coupled to said output pin
that provides said output pin with selectable
functionality in accordance with a type of memory.

15 24. The memory controller of claim 23
wherein said functionality of said output pin is one of
a chip select signal function and a clock signal
function.

20 25. A memory circuit comprising:
a plurality of memory modules, said
memory modules being of at least one type; and
a memory controller coupled to said
memory modules via a plurality of pins, at least one of
25 said pins having a selectable functionality based on
said type of said memory modules.

26. The memory circuit of claim 25 wherein
said selectable functionality comprises a clock signal
function.

27. The memory circuit of claim 25 wherein
5 said selectable functionality comprises a chip select
signal function.

28. A computer system comprising:
a central processing unit;
a memory controller coupled to said
10 central processing unit, said memory controller having
a plurality of input/output pins; and
a plurality of memory modules of at
least one type coupled to said memory controller via
said pins; wherein:
15 a subplurality of said pins has
selectable functionality, said functionality based on
said type of said memory modules.

29. The computer system of claim 28 wherein
said selectable functionality comprises a clock signal
20 function.

30. The computer system of claim 28 wherein
said selectable functionality comprises a chip select
signal function.

31. Apparatus for configuring a memory
25 controller, said memory controller having a plurality
of input/output pins, said apparatus comprising:

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means for informing said memory controller of a type of memory; and
means for configuring at least one pin of said memory controller to have a functionality in
5 accordance with said type of memory.

32. Apparatus for providing more than one function for an output pin of a memory controller, said apparatus comprising:

means for providing a clock signal
10 within said memory controller;
means for providing a control signal within said memory controller;
means for selecting within said memory controller one of said clock signal and said control
15 signal based on a type of memory; and
means for coupling said selected signal to said output pin.

33. A memory controller comprising:
at least one output pin;
20 multiplexer means for outputting one of at least two signals to said output pin;
signal means for selecting a chip, said signal means coupled to said multiplexer means;
control signal means coupled to said
25 multiplexer means; and
means coupled to said multiplexer means for selecting said control signal means based on a type of memory.

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34. A memory controller comprising:
at least one output pin;
multiplexer means having two inputs, a
control input, and an output coupled to said output
5 pin;
a clock signal coupled to one of said
two inputs;
a control signal coupled to the other
one of said two inputs; and
10 means coupled to said control input for
selecting one of said clock signal and said control
signal based on a type of memory.

35. A memory controller comprising:
at least one output pin; and
15 means for providing said output pin with
selectable functionality in accordance with a type of
memory.

36. A memory circuit comprising:
20 a plurality of memory modules, said
memory modules being of at least one type; and
memory controller means coupled to said
memory modules via input/output means, at least some of
said input/output means having a selectable
25 functionality based on said type of said memory
modules.

37. A computer system comprising:
central processing means;
memory controller means coupled to said

central processing means, said memory controller means having a plurality of input/output means;

a plurality of memory modules of at least one type coupled to said memory controller means
5 via said input/output means; wherein:

a subplurality of said input/output means has selectable functionality, said functionality based on said type of said memory modules.